REMARKS

The Office Action dated March 7, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

By this Amendment, claims 6 and 21 have been amended. Applicant submits that the amendments are fully supported in the Specification as well as the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1, 2 and 4-21 are pending in the present application and are respectfully submitted for consideration.

Claims 1, 2, 4, 5 and 16-18 were rejected under 35 U.S.C. §102(b) as being anticipated by Takahashi et al. (JP 40927070, hereinafter "Takahashi"). The applicant respectfully submits that each of claims 1, 2, 4, 5 and 16-18 recites subject matter that is neither disclosed or suggested by the cited prior art, and hereby traverse this rejection, as follows.

Claim 1 recites an input circuit having a current mirror circuit including a self-biased transistor and non-self-biased transistor connected to each other, and a differential circuit including a first transistor a first drain of which is connected to the non-self-biased transistor for receiving an external signal and a second transistor a second drain of which is connected to the self-biased transistor for receiving a reference signal. The first source of the first transistor and a second source of the second transistor are connected in common and have the same potential, and the differential circuit generates an internal signal at the first drain in accordance with a current flowing through the first and second transistors. The input circuit also includes a constant

current source connected to the first source of the first transistor, and a current regulating circuit connected to the second source of the second transistor and connected in parallel to the constant current source. The current regulating circuit increases and decreases an amount of the current flowing through the differential circuit in response to the internal signal wherein the internal signal is directly provided to the current regulating circuit.

Claim 16 recites an input circuit having a first MOS transistor having a gate that receives a data signal, and a second MOS transistor having a gate connected to a reference voltage. The source of the first transistor is connected to the source of the second transistor at a first node. The input circuit also includes a third MOS transistor connected between the first node and a low potential power supply, and having its gate connected to a high potential power supply, a fourth MOS transistor connected between the first node and the low potential supply, and a fifth MOS transistor connected between the drain of the first transistor and the high potential power supply. Furthermore, the input circuit includes a sixth MOS transistor connected between the drain of the second transistor and the high potential power supply. The gates of the fifth and sixth transistors are connected to each other and to the drain of the sixth transistor. Also, the input circuit includes a first inverter having an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor.

Accordingly, the present invention includes an input circuit wherein the internal signal is directly provided to the current regulating circuit, as recited in claim 1, and an input circuit having a first inverter having an input terminal connected to a second node

between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, as recited in claim 16. As such, the present invention results in the advantage of having an input circuit generating internal input signals which rise and fall in response to the rising edges and the falling edges of an external input signal.

The Applicant respectfully submits that each element recited within claims 1 and 16 is neither disclosed nor suggested by Takahashi. In particular, Applicant submits that the input circuit as claimed in the present application is clearly distinct from that which illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the features of an internal signal being directly provided to the current regulating circuit, and a first inverter connected to the gate of the fourth transistor. It is submitted that Takahashi merely discloses a transistor (P2 or N6), which is regarded as a current adjustment transistor by the Examiner, for receiving an internal signal (i.e., differential output signal) via a three stage inverter (DL1 or DL2). However, applicant respectfully submits that Takahashi fails to teach or suggest at least the limitation of the internal signal being directly provided to the current regulating circuit, as recited in claim 1. Accordingly, Applicant submits that the present invention, as recited in claim 1, is not anticipated by Takahashi.

Furthermore, Fig. 1 of Takahashi merely discloses a first MOS transistor (P3), a second MOS transistor (P4), a third MOS transistor (P1), a fourth MOS transistor (P2), a fifth MOS transistor (N1), a sixth MOS transistor (N2), and a first inverter (V1) having an input terminal connected to a node between the first and fifth transistors (P3, N1) and an output terminal connected to a delay circuit (DL1) and a second inverter (V2).

However, Applicant respectfully submits that Takahashi fails to teach or suggest at least the limitation of a first inverter connected to the gate of the fourth transistor (P2), as recited in claim 16. In other words, the first inverter (V1) is indirectly connected to the gate of the fourth transistor by the delay circuit (DL1). As such, Applicant submits that the present invention, as recited in claim 16, is not anticipated by Takahashi.

As for claims 2, 4, 5, 17 and 18, Applicant submits that as claims 2, 4 and 5 depend from allowable claim 1, and claims 17 and 18 depend from allowable claim 16, claims 2, 4, 5, 17 and 18 are likewise allowable.

Claims 1, 2, and 4-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fig. 1 of Applicant's admitted prior art ("AAPA") in view of Takahashi. AAPA was cited for disclosing many of the claimed elements of the present invention with the exception of showing the current regulating circuit and that the processing signal circuit includes a plurality of processing circuits. Takahashi was cited for allegedly curing this deficiency. The Applicant notes that claims 6 and 21 have been amended. The Applicant respectfully submits that each of claims 1, 2 and 4-21 recites subject matter that is neither disclosed nor suggested by the cited prior art, and to the extent that this rejection remains applicable to the claims, including claims 6 and 21, as amended, the Applicant respectfully traverse this rejection as follows.

Claim 6 recites a semiconductor integrated circuit having a plurality of input circuits. Each input circuit includes a differential circuit having a first transistor for receiving an internal signal having a first phase and a second transistor for receiving a reference signal. Sources of the first and second transistors are connected in common, in a differential circuit generate an internal signal having a second phase that is the

same as the first phase of the external signal in accordance with a current flowing through the first and second transistors. In addition, the input circuit includes a current regulating circuit, connected to the differential circuit, which regulates the amount of the current flowing through the differential circuit in response to the internal signal. The semiconductor integrated circuit also includes a plurality of complementary signal generating circuits, each connected to one of the input circuits. The complementary signal generating circuits receive the internal signal from the associated input circuit and generate a complementary signal of the input signal. Furthermore, the semiconductor integrated circuit includes a plurality of signal processing circuits connected to the plurality of complementary signal generating circuits, respectively. The signal processing circuits perform predetermined signal processing operations in accordance with the complementary signal.

Claim 21 recites a semiconductor integrated circuit for receiving a data signal in response to rising and falling edges of a data strobe signal having a first phase. The semiconductor integrated circuit includes a data strobe signal input circuit which receives the data strobe signal. The data strobe signal input circuit includes a differential circuit , a current mirror circuit, a constant current source, and a current adjustment transistor. The differential circuit has a first transistor and a second transistor to generate a differential output signal having a logic level and a second phase that is the same as the first phase of the data strobe signal, a first gate of the first transistor receiving the data strobe signal, a second gate of the second transistor receiving a reference signal, and sources of the first and second transistor being connected in common and having the same potential. The current mirror circuit

supplies a current to the differential circuit. The constant current source is coupled to the sources of the first and second transistor. And the current adjustment transistor is coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receives the differential output signal of the differential circuit. The current adjustment transistor turn ON and OFF in response to the logic level of the differential output signal such that a falling delay time and a rising delay time of the logic level of the differential output signal are substantially the same.

The Applicant respectfully submits that each element recited within claims 1, 6, 16 and 21 is neither disclosed nor suggested by AAPA and/or Takahashi, taking alone or in combination. In particular, it is submitted that AAPA fails to disclose at least the feature of a current regulating circuit, as claimed in claim 1. Furthermore and as commented above, Takahashi does not teach or suggest at least the limitation of directly providing an internal signal to the current regulating circuit, as claimed in claim 1. Accordingly, Applicant respectfully submits that claim 1 recites subject matter that is neither disclosed nor suggested in AAPA and/or Takahashi, taken alone or in combination, and therefore claim 1 is allowable over the cited prior art.

As for the rejection of claim 6, Takahashi fails to disclose at least the limitation of providing a differential output signal having a phase that is the same as a phase of an input signal (strobe signal), as claimed in claim 6, as amended. Specifically, as shown in Fig. 2 of Takahashi, when an input signal (Vin) rises from a low level to a high level, a signal (n3) provided to a transistor (P2) falls from a high level to a low level. In contrast, as a result of the present invention, as claimed in claim 6, as amended, as shown in Fig. 7, when an input signal (DQs) rises from a low level to a high level, a differential signal

(dqsz) also rises from a low level to a high level. Applicant respectfully submits that claim 6, as amended, therefore recites subject matter that is neither disclosed nor suggested in AAPA and/or Takahashi, take alone or in combination, and claim 6 is therefore allowable over the cited prior art.

With respect to claim 16, it is submitted that AAPA fails to disclose at least the limitation of a fourth MOS transistor connected between the first node and the low potential power supply and a first inverter haring an input terminal connected to a second node between the first and fifth transistors and an output terminal connected to the gate of the fourth transistor, as claimed in claim 16. It is further submitted that Takahashi does not teach or suggest at least the limitation of a first inverter connected to the gate of the fourth transistor. Therefore, Applicant respectfully submits that claim 16, therefore, recites subject matter that is neither disclosed nor suggested in AAPA and/or Takahashi, taken alone or in combination, and therefore claim 16 is allowable over the cited prior art.

As for claim 21, it is submitted that AAPA fails to disclose at least the limitation of a current regulating circuit, as claimed in claim 21, as amended. Moreover, Takahashi does not disclose at least the limitation of providing a differential output signal having a phase that is the same as a phase of an input signal (strobe signal), as claimed in claim 21, as amended. Accordingly, Applicant respectfully submits that claim 21 recites subject matter that is neither disclosed nor suggested in AAPA and/or Takahashi, taken alone or in combination, and therefore claim 21 is allowable over the cited prior art.

As for claims 2, 4-5, 7-15, 17-20, Applicant submits that as claims 2, 4, and 5 depend from allowable claim 1, and claims 7-15 depend from allowable claim 16, these claims are likewise allowable.

With regard to each of the rejections under §103 in the Office Action, it is also respectfully submitted that the Examiner has not yet set forth a *prima facie* case of obviousness. The PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 U.S.P.Q.2nd 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002).

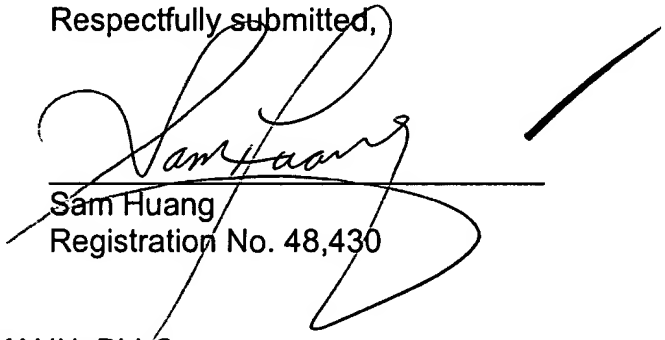
In view of the above, Applicant respectfully submits that claims 1, 2, 4-21, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the

claims not obvious to person of ordinary skill in the art, and therefore respectfully requests that claims 1, 2, 4-21 be found allowable and this application be passed issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, referencing docket number 108075-09014.

Respectfully submitted,



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